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P h y s i c s

DRIVER OUTPUT IMPEDANCE CALIBRATION SYSTEM WITH COMPARATOR UNIT OFFSET CANCELLATION

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In modern integrated circuits, the channel length of the transistors is reduced, and the supply voltages are also reduced. But the threshold voltages of the transistors cannot be reduced so quickly due to the physical properties of the materials used, which decreases the operating range of the transistors and makes noises comparable to them. Therefore, it is necessary to eliminate the influence of noise sources in the circuits, in particular, reflections between the transmission line and the output of the transmitter. A system is proposed for calibrating the output impedance of the transmitter based on an accurate external resistor with comparator unit offset voltage compensation. Existing analog and reference frequency based solutions have key disadvantages such as the inability to compensate the offset voltage after the integrated circuit is fabricated, and the distribution of the calibration voltage across the Input/Output device and constant power consumption during the operation. The proposed circuit includes a high-precision digital-to-analog converter to compensate the comparator offset voltage. It generates calibration codes for the pull-up and pull-down parts of the transmitter output buffer, and provides fine tuning of the output impedance. The circuit was modeled using 16 *nm* FinFET process elements and simulated with HSPICE simulator.

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***Keywords*:** Input/Output device, transmitter, reflection, transmission line, offset, output impedance.

Introduction. Integrated circuits are currently actively scaling and the number of elements per unit area is increasing. In the modern technological processes, the transistor channel length reaches to 3 *nm*. As the integrated circuits are scaled down, their operating voltages drop to 0.7 *V*, and the noise levels become comparable to the operating voltages [1–3]. But the threshold voltages of transistors, due to the physical properties of the materials used, cannot be reduced in the same proportion as the supply voltages. Therefore, the difference between the transistors' supply and

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threshold voltages decreases, by that reducing the operating range of the transistors and, consequently, the noise immunity. Along with the aforementioned circumstances, the operating frequencies of integrated circuits increase, due to which the physical parameters of the transmission lines change. For the above reasons, it is currently very important to maintain the independence of operating parameters from the side effects of integrated circuits, in particular, Input/Output devices.

The main factors limiting the operating frequency of integrated circuits are the Input/Output devices (as they use relatively slow thick-oxide transistors) and the transmission lines, connecting the Input/Output devices to other parts of the system. A mismatch between the transmitter output and receiver input impedances at the beginning and at the end of the transmission lines can lead to false logical switching or resist to the establishment of a logically correct state. In order to avoid reflections, the impedances of the transmission line, transmitters' output and receivers' input should be as close as possible.

In order to calibrate the impedances, a reference parameter is needed to obtain the desired nominal value by comparing the new value with the reference. The main modern methods of impedance calibration are the analog calibration system based on external precise resistor and the mixed-signal calibration system using the reference frequency [4–7]. The essence of the operation of an analog calibration system, based on precise resistor outside the integrated circuit, is to get equal voltage drops across that resistor and the transmitter output buffer. It is implemented by a feedback operational amplifier, the output of which gives a bias voltage for the gates of output buffer transistors of transmitter. This method has two main disadvantages. The output analog voltage of the operational amplifier must be distributed throughout the Input/Output device to transmitters, and it is very sensitive to noise. Also the system must always be switched on during the whole operation of the integrated circuit and therefore consumes a lot of power. The operation of the mixed-signal calibration system using the reference frequency is based on the fact that the output signal frequency of the voltage-controlled oscillator varies with changes in the process voltage and temperature. The output voltage of a high-frequency voltage-controlled oscillator is passed through the divider and compared with the reference frequency (obtained from a quartz generator), resulting in a calibration code (set of voltages applied to the transistor gates) for the output buffer for all transmitters of Input/Output device. In that case, the system generates the calibration code once during the mission mode but cannot control the frequency drifts during the operation.

Considering the shortcomings of the existing solutions, a mixed-signal system for calibration of the transmitter output impedance is proposed, which is based on a high-precision resistor outside the integrated circuit, in which a comparison block (in this case, clocked amplifier) offset voltage cancellation mechanism is embedded, to eliminate process, voltage and temperature variations after the production.

Concept of the Proposed Method. The proposed mixed signal system for calibrating the output impedance of the transmitter consists of three main parts: replica cells of the output buffers of the transmitters, a digital finite state machine, and

a mixed signal comparison block (Fig. 1). Outside the integrated circuit, there is a high-precision reference resistor with which the transmitter output buffer's pull-up and pull-down resistances should be compared. The main advantage of the system is that the offset voltage of the comparator circuit is cancelled due to the high-precision digital-to-analog converter (DAC) in the mixed-signal comparison block.

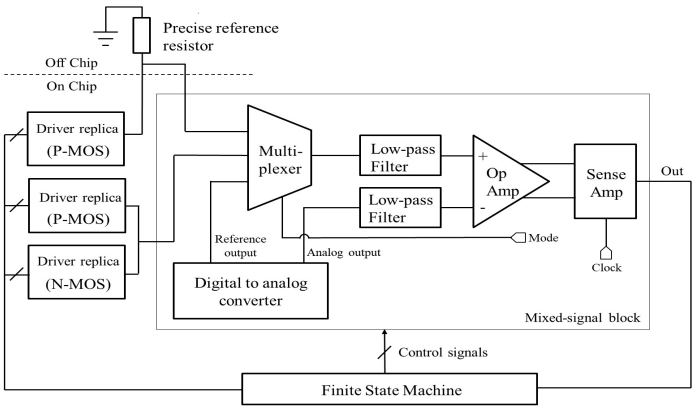

Fig. 1. Transmitter output impedance calibration mixed signal system block diagram.

The whole calibration system is controlled by the finite state machine. It is a completely digital circuit described in Verilog or another hardware description language. It generates all the necessary control signals for the calibration system, as well as changes the DAC input code and determines the operating mode of the circuit "mode" input). At the initial stage of the circuit operation, the offset voltage of the comparator unit is canceled.

With the "mode" input, which is the multiplexer selection input, the reference output of the DAC is selected, which connects to the positive input of the operational amplifier. The negative input is connected to the analog output of the DAC. Low-pass filters are connected to the inputs of the operational amplifier to filter high frequency noises. A DAC with a resistance ladder architecture is chosen, with coarse and precise ladders, which ensures accurate offset voltage cancellation. A voltage equal to half the supply voltage of the Input/Output device is connected to the reference output. The finite state machine with a built-in search algorithm begins to change the DAC code (hence the DAC output analog voltage), starting from the middle point, until the "out" output is toggled. The voltage corresponding to the given code will be fixed on the negative input of the operational amplifier as a reference voltage for further comparisons. With the above step, after the production of the integrated circuit, it is possible to cancel the offset voltage of the operational amplifier for more accurate impedance calibration. The positive and negative outputs of the operational amplifier are connected to a clocked sense amplifier, based on a latch circuit. By that, even if a small voltage difference is present on the operational amplifier outputs, the sense amplifier output will switch. Sense amplifier is designed to be clocked, so that the circuit could be used in synchronous environments.

After offset voltage cancellation step, it is necessary to obtain the calibration codes for the transmitter output buffer pull-up and pull-down parts. For this purpose, by changing the "mode" signal (multiplexor selection input), the pull-up part of the replica driver output buffer is selected, so that it forms a voltage divider with the reference resistor outside the integrated circuit. Since the negative input of the operational amplifier already has a voltage of about half of the supply voltage (already with cancelled offset), the pull-up resistance of the transmitter output buffer after the comparison will be equal to the reference resistance. The finite state machine then changes the transmitter pull-up calibration code, with the built-in search algorithm, until the "Out" output is switched, which means that operational amplifier inputs have got equal. The obtained code will be the pull-up calibration code of the transmitter output buffer. The next step is to adjust the driver output buffer pull-up resistance, which should be compared to the already calibrated pull-down part. By changing the "mode" signal, a replica is selected with the pull-up and pull-down parts, which form a voltage divider. The finite state machine sets the calibration code to transistors' gates for pull-up part and changes the pull-down code until the "Out" output is switched, which means that the pull-up and pull-down resistances are already equal. As a result, we get calibration codes for the transmitter output buffer pull-up and pull-down parts, which are transferred to all Input/Output device drivers for current mission mode operation.

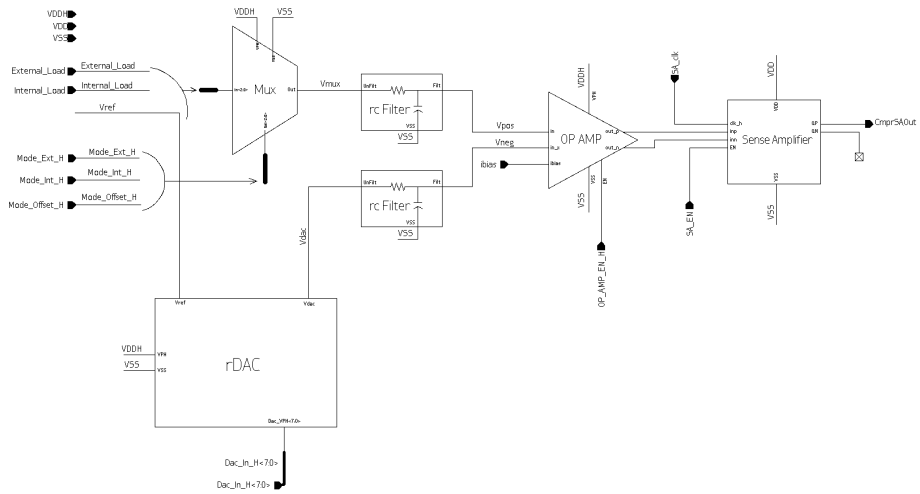

Fig. 2. Transmitter output impedance calibration system's mixed-signal block.

The nominal value of the external high-precision reference resistance, and therefore the output impedance of the transmitter, is determined in accordance with the technical specification and applicable standards. The drawback of the proposed architecture is that it occupies a large area on the integrated circuit, due to a large resistor ladder based precise DAC and replicas of the transmitters.

Implementation of the Proposed Circuit. Transmitter output impedance calibration system's mixed-signal block is presented in Fig. 2. It includes resistor

ladder based DAC (rDAC), multiplexer (Mux), low-pass filter (rc Filter), operational amplifier (OP AMP), clocked sense amplifier (Sense Amplifier). All circuits are under the supply voltage of Input/Output device, except for the sense amplifier, as its output is connected to the digital finite state machine, which is located in the core.

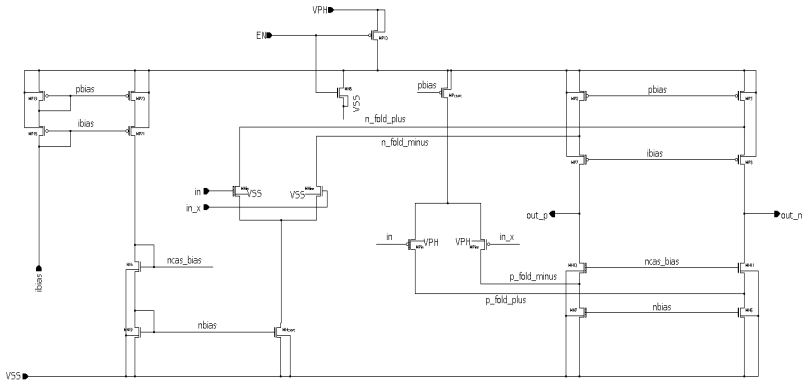

Fig. 3. Operational amplifier circuit.

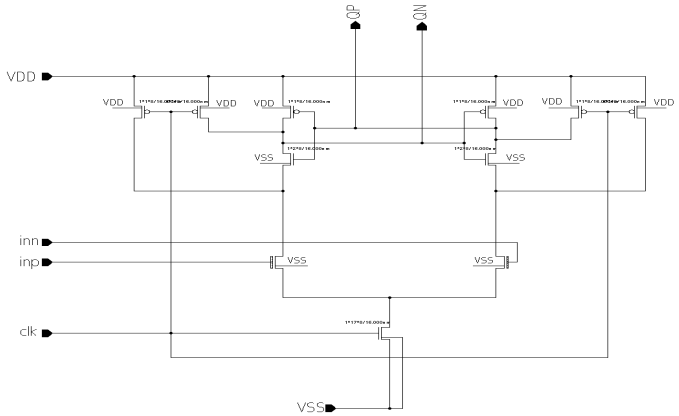

Fig. 4. Clocked sense amplifier circuit.

The rail-to-rail architecture was chosen for the operational amplifier, as one of its inputs is connected to the output of the DAC, the other input is connected to a voltage divider, and they receive a wide-swing voltage signals (Fig. 3). This architecture ensures the saturation mode of the input transistors of the operational amplifier at all possible input voltages.

The sense amplifier is a clocked latch (Fig. 4). When the clock signal is low, the circuit is disconnected from the ground and the remaining points of the circuit are connected to the power supply, indicating that the circuit is in the non-operating mode. With a high clock signal, the circuit operates based on a latch with two cross-connected inverters, and in case of a small change at its inputs, the output switches.

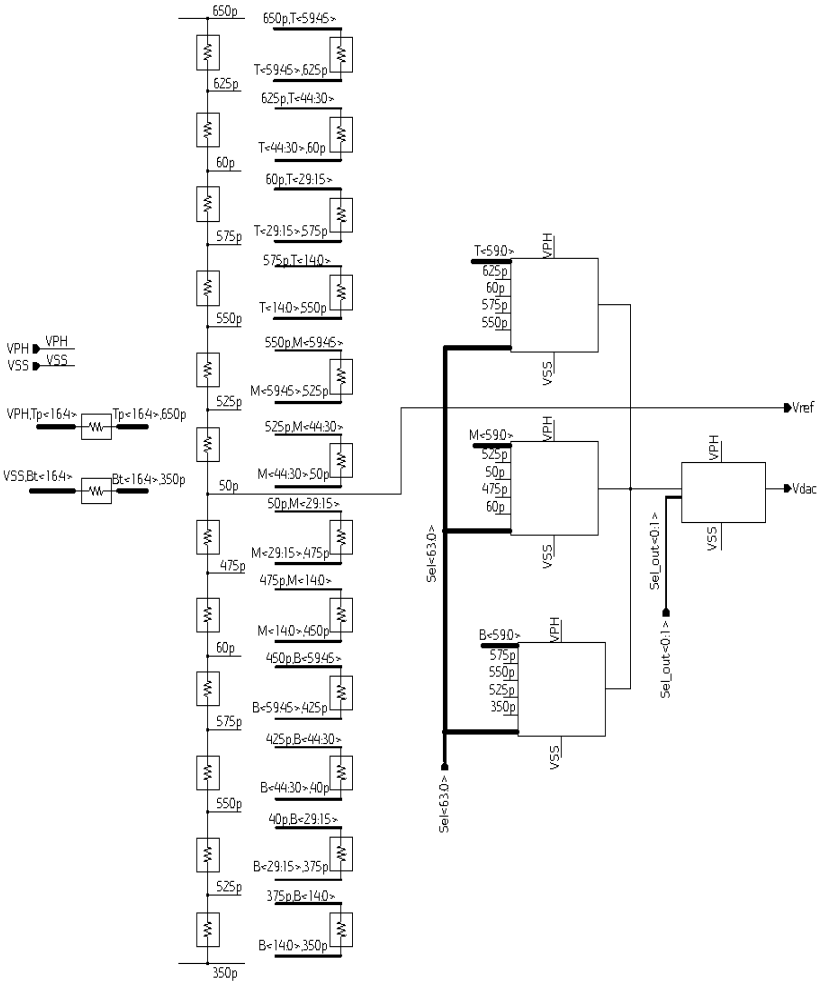

Fig. 5. Resistor ladder-based DAC circuit.

The DAC is the main part of the calibration system being responsible for the accuracy of the calibration (Fig. 5). A resistor ladder based DAC has been chosen because it provides high accuracy and high linearity compared to other architectures, which is necessary to cancel the offset voltage of the operational amplifier as well as to ensure a small step of the output voltage. 8-bit decoder is used in DAC, and the series of resistors are divided into two parts: coarse and precise resistor ladders, which are connected to the output by transmission gates. The lower and upper limits of the conversion range are respectively 35% and 65% of the supply voltage. The conversion range is divided into 13 levels by 12 resistors including the endpoints (coarse ladder) and each range is in turn subdivided by 16 resistors (precise ladder), resulting in the least significant bit (LSB) being 0.156% of the supply voltage. The voltage corresponding to 50% of the supply voltage is also taken out with a separate output pin to act as a reference voltage during the offset voltage.

The multiplexer is designed for three inputs with a three-bit selection input. It is

implemented with transmission gates. The low frequency filter has a simple structure: resistance and grounded capacitance.

Simulation Results. The proposed circuit is constructed using 16 *nm* FinFET technological process and both thick- and thin-oxide transistors. The supply voltage of the Input/Output device is 1.2 V and the core voltage is 0.9 V, which are the nominal voltage values for the above types of transistors. The simulations were performed using HSPICE simulator [8]. The circuits were tested for typical, slow and fast process cases, for $\pm 10\%$ voltage values and for temperature range of -40 to 125°C and for all possible combinations of the above parameters.

The following parameters have been tested for the proposed circuit: low-pass filter cut-off frequency, DAC output voltage range, as well as differential and integral nonlinearity, operational amplifier gain, phase margin and frequency bandwidth, comparator (operational amplifier and sense amplifier together) offset voltage, delay from clock signal to output. AC analysis was performed to determine the cutting frequency of the filter. To determine the DAC parameters, transient analyses were carried out by changing the 8-bit input code from the lowest to the highest. Differential and integral nonlinearity values were calculated for all codes and the worst cases were picked. AC analyses were performed to determine the parameters of the operational amplifier. To define the offset voltage of the comparator, a DC analysis was performed, calculating the difference of the inputs when the output is switching (one of the inputs is connected to the 50% of support voltage, the other is sweeping). A transient test was performed to determine the delay from the active front of the comparator clock signal to the output. The following table shows the simulation results.

Simulation results

Parameter	Unit	Min. value	Max. value
Filter cut-off frequency	*MHz*	19.4	41.6
DAC output voltage range	Supply voltage, %	35.47	64.51
DAC differential nonlinearity	Supply voltage, %	–	0.16
DAC integral nonlinearity	Supply voltage, %	–	0.11
Operational amplifier gain	*dB*	40.2	68.6
Operational amplifier phase margin	degree	53.9	64.1
Operational amplifier frequency bandwidth	*MHz*	426	825
Comparator offset voltage	*mV*	4.87	7.41
Comparator clock to output delay	*pS*	101	254

Conclusion. A system for calibrating the output impedance of the transmitter is presented based on a precision off-chip reference resistor with offset compensation of the comparator. Existing analog and reference frequency based solutions have key drawbacks such as the inability to compensate the offset voltage after the integrated circuit is fabricated, the distribution of the calibration voltage across the Input/Output device, and constant power consumption during operation. After powering up the integrated circuit with a high accuracy digital-to-analog converter and finite state machine, the offset voltage of the comparison unit is canceled, which ensures accurate

calibration of the output impedance of the transmitter. The drawback of the proposed architecture is that it occupies a large area on the integrated circuit due to a large resistor ladder based precise DAC and replicas of the transmitters.

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Վ. Ս. ԳԵՎՈՐԳՅԱՆ

ՀԱՂՈՐԴՉԻ ԵԼՔԱՅԻՆ ԴԻՄԱԴՐՈՒԹՅԱՆ ԿԱՐԳԱԲԵՐՄԱՆ ՀԱՄԱԿԱՐԳ՝ ՀԱՄԵՄԱՏՈՂ ՀԱՆԳՈՒՅՑԻ ՇԵՂՄԱՆ ԼԱՐՄԱՆ ՉԵՂԱՐԿՄԱՄԲ

Արդի ինտեգրալ սխեմաներում փրանզիստորների հոսքուղու երկարությունը նվազում է, ինչպես նաև նվազում են սնման լարումները: Բայց փրանզիստորների շեմային լարումները չեն կարող նվազել նույնքան արագ օգտագործվող նյութերի ֆիզիկական հատկություններից ելնելով, ինչի պատճառով փրանզիստորների աշխատանքային լարման միջակայքը նվազում է, և աղմուկները դառ-

նում են համեմատելի նրանց հետ: Այդ պատճառով հարկավոր է բացառել աղմուկների աղբյուրների ազդեցությունը շղթաներում, մասնավորապես անդրադարձումները՝ հաղորդիչ հանգույցի ելքի և փոխանցման գծի միջև: Առաջարկվում է արտաքին ճշգրիտ հենակային դիմադրության վրա հիմնված հաղորդչի ելքային դիմադրության կարգաբերման համակարգ՝ նրանում գտնվող համեմատող հանգույցի շեղման լարման չեղարկմամբ: Առկա անալոգային և հենակային հաճախության վրա հիմնված լուծումներն ունեն առանցքային թերություններ, որոնք են ինտեգրալ սխեմայի արտադրությունից հետո շեղման լարման չեղարկման անկարողությունը, ինչպես նաև կարգաբերման լարման տարածումն ամբողջ մուտք-ելք սարքով, աշխատանքի ընթացքում անընդհատ էներգասպառումը: Առաջարկվող շղթան ներդրված բարձր ճշտությամբ թվա-անալոգային կերպափոխիչի և վերջավոր վիճակների ավտոմատի շնորհիվ չեղարկում է համեմատիչի շեղման լարումը և գեներացնում կարգաբերման կոդեր՝ հաղորդչի ելքային բուֆերի վերև և ներքև քաշող մասերի համար, ինչն ապահովում է ելքային դիմադրության ճշգրիտ կարգաբերում: Շղթան մոդելավորվել է 16 *նմ* FinFET տեխնոլոգիական գործընթացի տարրերով և HSPICE ծրագրային միջոցով:

В. С. ГЕВОРГЯН

СИСТЕМА КАЛИБРОВКИ ВЫХОДНОГО ИМПЕДАНСА ПЕРЕДАТЧИКА С АННУЛИРОВАНИЕМ СМЕЩЕНИЯ СРАВНИТЕЛЬНОГО УЗЛА

В современных интегральных схемах длина канала транзисторов уменьшается, а также уменьшается напряжение питания. Но пороговое напряжение транзисторов не может быть уменьшено так быстро из-за физических свойств используемых материалов, из-за чего рабочий диапазон транзисторов уменьшается и шумы становятся сравнимыми с ними. Следовательно, необходимо исключить влияние источников шума в цепях, в частности отражения между линией передачи и выходом передающего узла. Предлагается система калибровки выходного сопротивления передатчика на основе точного внешнего резистора с аннулированием напряжения смещения узла компаратора в нем. Существующие аналоговые решения и решения на основе опорной частоты имеют ключевые недостатки, такие как невозможность нейтрализовать напряжение смещения после изготовления интегральной схемы, а также распределение напряжения калибровки по устройству ввода/вывода и постоянное энергопотребление во время работы. Предлагаемая схема включает высокоточный цифро-аналоговый преобразователь для нейтрализации напряжения смещения компаратора, генерирует коды калибровки для верхней и нижней части выходного буфера передатчика и обеспечивает точную настройку выходного сопротивления. Схема была смоделирована с использованием элементов 16 *нм* FinFET технологического процесса и программным обеспечением HSPICE.